Architecture of data-acquisition systems for high-energy physics experiments

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In this review we discuss the evolution of the basic principles of the architecture of data-acquisition systems for experimental setups used in high-energy physics and relativistic nuclear physics during the last 25 years. The effect of the latest advances in computational techniques and communications, such as microprocessors and open bus system standards, on improving data recording and acquisition is discussed. The evolution of data-acquisition systems is illustrated by examples of developments occurring at the leading physics centers and at the Laboratory of High Energy Physics, JINR, Dubna. The trends in the future development of data-acquisition systems are described for the research programs at the LHC collider, CERN, and the Relativistic Heavy Ion Collider at Brookhaven National Laboratory. [S1063-7796(97)00105-8]

INTRODUCTION

The experimental research currently being carried out in high-energy physics and relativistic nuclear physics focuses on the study of processes which occur with very low probability against the background of processes more probable by several orders of magnitude. Even an experimental setup which contains relatively few detectors and which is designed for such research involves several hundred thousand data channels. This determines the volume of the electronic apparatus which is needed to organize the data-acquisition (DAQ) systems. These systems are based on nuclear electronics modules, computing devices, including computers and computing modules realized in some standard (CAMAC, VME, FASTBUS, etc.), and also computer interfaces. During the last 25 years, devices for recording experimental data have been developed particularly quickly, largely because of the latest advances in computational techniques and means of communication.

The experimental installations used in high-energy and relativistic nuclear physics are designed to conduct experimental studies at charged-particle accelerators. As a rule, the operating time for an experimental setup at an accelerator is severely limited. This makes it necessary to construct high-performance DAQ systems which allow the recording of a sufficient number of events of the physical process under study in the minimum possible time of exposure at an accelerator. Therefore, the main task of DAQ systems is to record the maximum possible number of useful events. This mainly depends on the efficiency of event selection and the time needed to read the data on the event, which in turn depend on the design (architecture) of the DAQ system.

Analysis of the architecture of the various DAQ systems operating in high-energy physics shows that they have much in common. The main differences reflect the specific features of the physical processes studied and the detectors used.[1]

The experimental installations at the JINR are designed by a broad international collaboration, which makes it necessary to use a *standard* approach for designing all the hardware and software components of the DAQ systems. Analysis of the experience with constructing DAQ systems over the last 25 years shows that the efficiency of an entire system mainly depends on its architecture. The main principles of the architecture of DAQ systems currently mentioned most often in the literature are the following:

1. A *unified architecture*, i.e., the capability of combining all the hardware needed for data recording into a single aggregate. *Upgradability* of the system, i.e., the possibility of incorporating new devices into it, is also important, as is *expandability*, so that enlargement of the system can be achieved by simply connecting new elements to the system buses.

2. A *modular* and *open* design, which ensures that the requirements of various experiments can be met. This allows the requirements to be changed in the course of operation of the system, which ensures independence of the specific supplier of the electronic modules, and which guarantees that the apparatus can be used for future-generation experiments.

The architecture of a DAQ system is based on the following:

1. *Coupling* and *interface* elements, which provide the needed *communications* between the master and slave modules of the data-transfer system, information exchange, and the transfer of urgent signals. In particular, they determine the transmission capability of the coupling channels, and also the width of transmitted address and data codes. Processor nodes and computers are incorporated into the system via them, and they form the basis of the multiprocessor system.

2. *Processor(s)* and/or *computers*, which control the data acquisition process, perform preliminary processing (compression, filtering, inclusion of calibrations, preliminary analysis) of the experimental data, decide whether or not it is suitable to accept data on an event, and ensure dialog with the human operator, visualization of the data acquisition process, and data transfer to long-term storage devices. The processor elements must operate with high performance, they must be capable of integration into the DAQ system, and they must ensure the possibility of operation in real time and as part of a multiprocessor system.

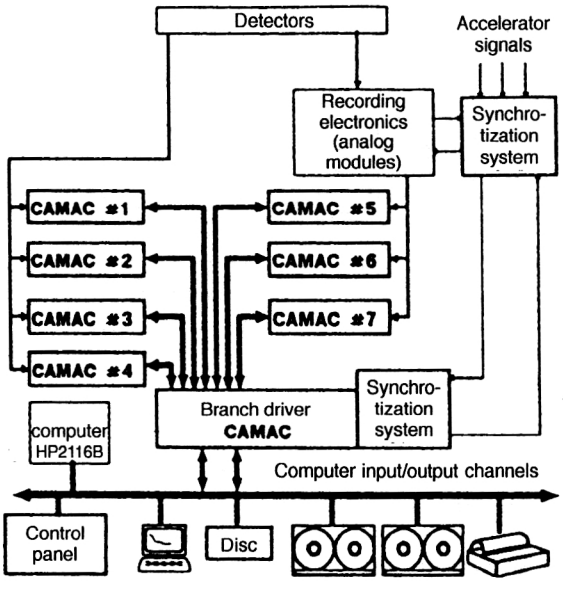

FIG. 1. Block diagram of the DAQ system of the FOTON setup based on the HP2116B minicomputer.

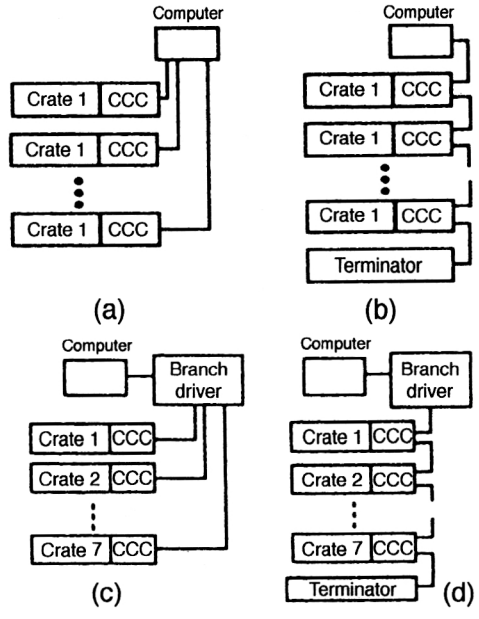

FIG. 2. Architecture of the main types of hardware-based DAQ system in the CAMAC standard.

2. STAGES IN THE DEVELOPMENT OF DAQ-SYSTEM ARCHITECTURE

2.1. Single-processor systems

In the late 1960s and early 1970s it became impossible to perform experiments in high-energy physics without using small computers in DAQ systems.[2] The computer became a fundamental component of the experimental setup, just like particle detectors and nuclear electronics modules.

A small computer was first used at the JINR Laboratory of High Energy Physics to organize the data acquisition from a setup designed to study radiative decays of resonances (the FOTON setup).[3] The Hewlett–Packard HP2116B was first used. This small computer had a rather simple set of commands, with an execution time of about 1 μsec. The 32-K RAM of 16-bit words was used to store programs, data buffers, histograms, and other experimental results. The use of only a single processor in the experimental setup was dictated by both operational requirements (a single computer was sufficient for the rate of data acquisition in the experiments) and financial reasons (the cost of the computer system essentially determined the cost of the entire setup). The number of data channels of the FOTON setup exceeded the number of input/output (i/o) channels of the computer to which devices could be connected. This problem was solved by using devices in the CAMAC standard with the creation of the corresponding interfaces to the i/o channel of the computer.[4,5] In Fig. 1 we show the block diagram of a typical single-processor DAQ system.

At that time the construction of DAQ systems for experimental setups encountered two fundamental methodological problems:[6]

- Combination of the devices associated with the many recording channels and arranged in several CAMAC crates to form a single system;
- Design of interfaces for coupling recording devices to the i/o channel of the computer controlling the data acquisition.

In Fig. 2 we show examples of the architecture of the basic types of DAQ system designed to solve these problems.[7–9] These are multicrate systems based on specialized CAMAC crate controllers (CCCs) designed to operate with a particular type of computer. In Fig. 2a we show the radial connection of the CCCs, where each crate is a single peripheral device mounted on the computer i/o busbar.[10,11] At the JINR Laboratory of High Energies this type of connection was used in designing the first stages of the DAQ system of the FOTON setup.[12] In Fig. 2b we show the loop connection of the controllers to the i/o channel of the computer.[13,14] In Fig. 2c we show the connection using a specialized CAMAC branch driver.[15] The development of such a specialized driver for the HP2116B computer made it possible to create a multicrate DAQ system for the FOTON setup,[16] allowing the experimental study of the differential cross sections for reactions of the type $\pi^- p \to \eta n$ at momentum 3.3 GeV/c (Ref. 17). The creation of the standard for constructing the CAMAC branch,[18] which also determined the operating principles of the Type-A crate controller (ACC) led to the development of DAQ systems with the architecture shown in Fig. 2d (Refs. 19 and 20).

The use of a CAMAC branch driver specialized for a given type of small computer proved very promising, especially for the architecture of small (2–4 CAMAC crates) DAQ systems. Only a few years ago this device was used as the basis for designing several setups at the JINR Laboratory of High Energies. In Fig. 3 we show the block diagram of the automated trigger control system of a streamer chamber,[21] and in Fig. 4 we show the block diagram of the SPHERE setup for experiments to search for the production of cumulative muon pairs with small invariant mass.[22]

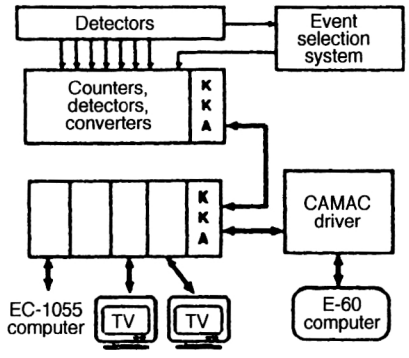

FIG. 3. Block diagram of the automated trigger control system of a streamer chamber.

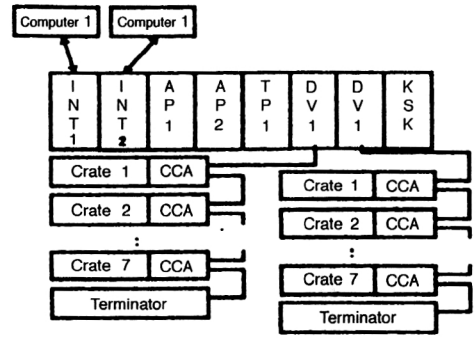

FIG. 5. Block diagram of a CAMAC system crate.

2.2. Centralized multiprocessor systems

In the second half of the 1970s, because of (a) the appearance of new types of detector, (b) the increased complexity and volume of devices, and (c) the need to record large data flows, it became essential for experiments to design DAQ systems containing several sources of control.[23] The use of such systems led to a great improvement in the quality of experiments, as they could perform real-time (1) preliminary data processing and compression, (2) event filtration in order to improve the ratio of potentially interesting events to the number of background events and increase the rate of recording useful events, (3) calibration and control during the operation of the recording devices, and (4) fast feedback to the experimentalist in the case of breakdown or equipment malfunction. Preprocessing of the input data was needed to speed up the later processing. It became possible to correct data by subtracting pedestals, taking into account enhancement factors, calibration constants, and coordinate transformations, and also to perform compression or rearrangement of the data by suppressing null information and inserting markers. The preprocessing required the introduction of additional processors distributed throughout the DAQ system, thus creating the prerequisites for the appearance of the *multilevel event-selection technique.*

This led to the necessity of creating DAQ systems which would allow, first, the connection of more than one standard CAMAC branch (7 crates) to a computer, second, simple changeover from one type of controlling computer to another, and, third, the introduction of several control sources into the system.

A device called a CAMAC system crate was developed in several laboratories. An original type of system crate was developed at the Laboratory of High Energy Physics.[24] The importance of this work was attested to by the nearly simultaneous appearance in the world-wide market of nuclear electronics modules of two types of system crate made by GEC Elliott Automation Ltd.[25] and Nuclear Enterprises Ltd.[26] The three devices were of different construction. In contrast to the designs from the West, the system crate of the Laboratory of High Energies did not require the use of an additional hanging bus, and had a large number of control sources (up to 20) and CAMAC branches (up to 10).

A system crate (see Fig. 5) is a multiprocessor system. Its operation can be controlled via computer interfaces (INT), single-chip computers (CPU), and autonomous processors (AP) with fixed algorithm for processing the input information. Since all the control elements of the system crate are concentrated at a single level, the system remains centralized. The performance of this system can be improved by:

- Simultaneous access to the readout data through the processor element controlling the readout process, and through one or several processor devices operating in the mode of capture of data transferred along the bus between master and slave devices;
- A conveyer mode involving several control elements, when the phase of data-word readout from the conversion cycle to the recording apparatus of one of the devices coincides in time with the phase of preparation of the corresponding conversion cycle of another device;
- The simultaneous performance of several experimental tasks by a set of processors.

The system crate developed at the Laboratory of High Energy Physics was used as the basis for:

- A system for automatic measurement and control of the parameters at the proton synchrotron[27] (see Fig. 6);
- Data-acquisition systems for the experimental setups (see Fig. 7) BIS-2 (Ref. 28), Alfa (Ref. 29), Kristall (Ref. 30), SYaO (Ref. 31), and DISK-2 (Ref. 32);
- An automation system for the booster synchrotron at IHEP in Protvino.[33]

The use of the system crate ensured that the automation

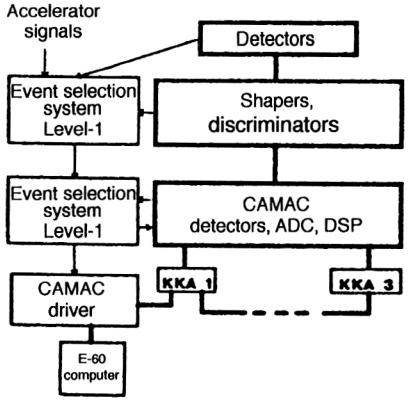

FIG. 4. Block diagram of the first stage of the experimental setup SPHERE.

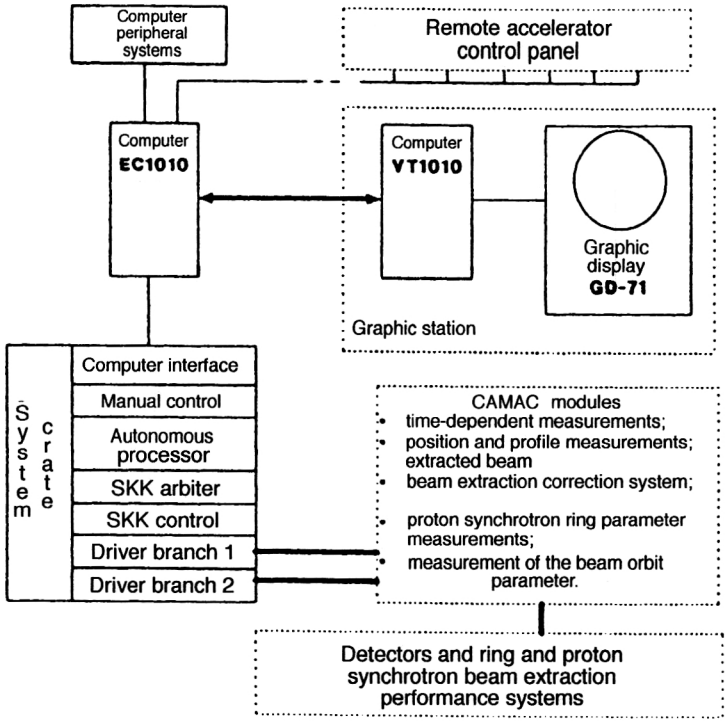

FIG. 6. The role of the system crate in controlling the parameters of the system for slow beam extraction from the synchrophasotron.

system possessed the properties of *modularity*, *upgradability*, and *openness*. This made it easy to modernize the DAQ systems based on the system crate designed at the Laboratory of High Energy Physics.

In spite of all the improvements, the CAMAC standard limited the further development of DAQ systems. The chip size in many cases was too small, and the power supply and mechanical constructions were too expensive. The standard was originally designed and optimized for systems involving a single control source, essentially ensuring expansion of the i/o system of a computer. Even the concept of system crate was limited due to the small address space and low throughput (from 0.5 to 2 Mbyte/sec in block transfers).

2.3. Multiprocessor systems with distributed computing resources

The appearance of microprocessors and the FASTBUS and VME standards used to construct multiprocessor 32-bit open bus systems solved the problem of high-speed communications (up to 80 Mbyte/sec), the capacity problem (up to 4 Gbytes of addresses), and also the problem of links between processors. It also led to the development of the architectural concept of multiprocessor DAQ systems[34] with distributed computing resources. Devices in the CAMAC, VME, and FASTBUS standards were used to construct DAQ systems. Most DAQ systems in high-energy physics had a tree struc-

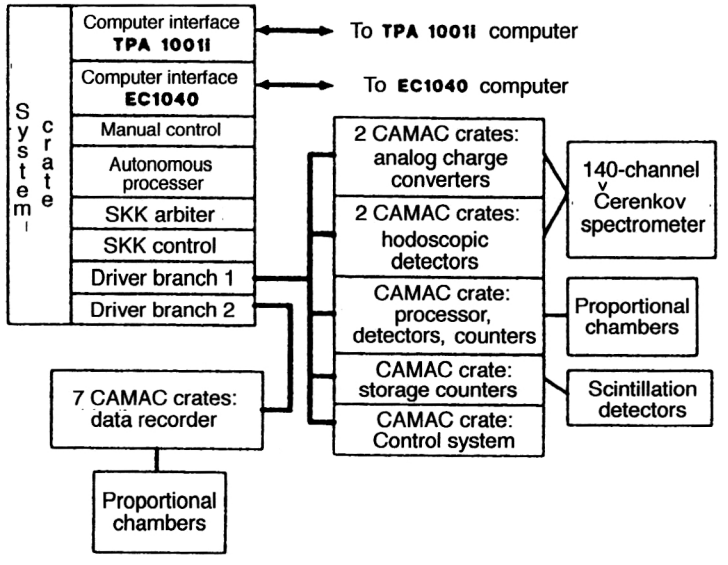

FIG. 7. Architecture of the DAQ system for the BIS-2 setup based on the system crate.

ture containing a large number of processors at all levels. The information about an event in such a system consists of data sets, each describing a process recorded by an individual detector or a group of detectors in the setup. The event information is sent via DAQ channels in a single defined direction and subjected to various operations along its route: filtering, shaping, compression, monitoring, choice of transfer path, and so on. These operations are performed by a set of processors distributed throughout the tree structure of the DAQ system. Processors of extremely diverse types operate under the control of various operating systems and are combined into a single system by means of standard buses like CAMAC, VME, FASTBUS, etc. To maximize the efficiency, the processors and memories are distributed throughout the system such that the individual branches and levels of the system can operate in parallel. In this system the individual modules obey master–slave relations.

Further advances in the technology of open bus systems and microprocessors requires the development of DAQ systems in which the modules are connected in the form of a network with client–server relations between them.[35] Such systems are characterized by the highly organized parallel operation of many processors.

3. METHODS OF CONSTRUCTING DAQ SYSTEMS

3.1. Open bus systems

The architecture of DAQ systems is in many respects determined by open bus systems. The standards of open bus systems[36] were developed to effectively support interprocessor interactions. A single bus connects processor modules, memory modules, and peripheral modules, ensuring arbitration by a control module, access to the address space specified by a 32-bit address code, exchange of 32-bit data, and operation via interrupt signals. The use of devices in these standards for constructing DAQ systems solves the problem of combining all the recording electronics within a single complex and also provides organization of communications and links between the processors and other system elements.

Most open bus systems are based on the EUROMECHANICS standard, which determines the construction principles for the supporting mechanical structures, the 19-inch installation (482.6 mm). The size of the basic module is 100× 100 mm, and it can be increased in steps of 60 mm in depth and 133.35 mm in height.

Until now, the FASTBUS and VME standards, along with some some standards which augment and extend the VME standard, have been widely used in the architecture of DAQ systems. Moreover, a number of new standards for high-speed open bus systems have been developed (FUTUREBUS+, SCI, Fiber Channel, HIPPI, ATM) for developing high-performance DAQ systems, and also for the transfer and switching of large amounts of data. Of these, FUTUREBUS+ and SCI are in the stage of discussion and creation of mock-up systems, while Fiber Channel, HIPPI, and ATM are already in use.

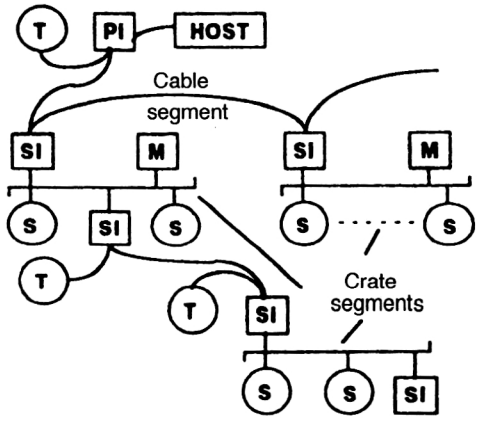

FIG. 8. Topology of systems in the FASTBUS standard.

3.1.1. FASTBUS

The FASTBUS standard is designed for the creation of large multiprocessor, multiaddress DAQ systems.[37] The basic element of the standard is a segment: an autonomous bus connecting a set of master [M] and slave (S) modules (see Fig. 8). There is a crate segment and a cable segment. A [SI] module is used to connect segments. The data and address transfer occur via 32-multiplexed bus lines.

The FASTBUS highway ensures data transfer in the single-transfer mode at a rate of up to 35 Mbyte/sec, and in the block-transfer mode at a rate of up to 70 Mbyte/sec. Because of the large size of the printed circuit board (366.7× 400 mm), the low-noise, high-power (up to 1950 W) power supply, and also the wide range of voltages, the FASTBUS standard is mainly used for precision multichannel analog modules of recording electronics, for example, a 96-channel ADC, a 64-channel TPD, and so on. In addition, there are a number of high-performance single-chip processor modules in the FASTBUS standard for managing data readout and fast preprocessing.[38]

3.1.2. VME standard

The VME standard[39] is used for the creation of high-performance multiprocessor computing systems of the modular type based on a unified highway. Data exchange occurs via a 32-bit busbar. The addressing is also done using 32-bit code, which ensures access to 4 Gbytes of memory. The data and address lines are separated. Asynchronous data-transfer protocol is used on the VME busbar, which implies the absence of a central data-transfer coordinator. The data-exchange rate is determined by the slowest module participating in the transfer. Control modules in the VME standard are being studied; examples are processor and peripheral modules allowing operation via a direct memory access (DMA) channel, and slave modules such as memory and i/o modules.

There are many examples of the use of the VME standard for constructing DAQ systems based on a VME crate as the central element of the system. The crate highway is designed to unify and ensure the simultaneous operation of

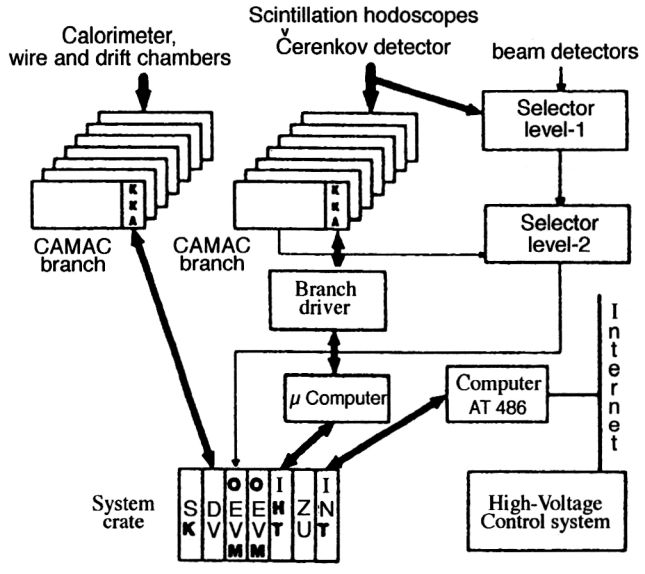

FIG. 9. Use of a VME system crate for organizing the DAQ system of the SPHERE setup.

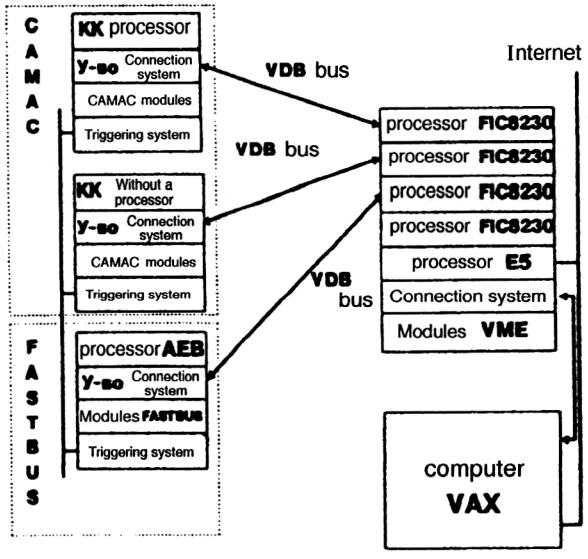

FIG. 10. Block diagram of a DAQ system with electronics in various standards connected via a VDB.

several processor devices. The insertion of at least one processor element in each electronics cluster pertaining to an individual detector allows information to be recorded simultaneously via several parallel branches. One of the processors acts as the central one. It synchronizes the operation of all the elements of the system as they collect data on an event and builds the complete event on the basis of the information from the individual subsystems. Such a system can include processors which perform an express analysis of the data directly in the course of the experiment and also graphically represent the information obtained, which aids the operational control during the experiment.[40]

As an example, let us consider the DAQ system of one of the stages of development of the SPHERE setup at the JINR Laboratory of High Energy Physics.[41,42] It was necessary to take a new approach to the design of the DAQ system due to the requirements of organizing data acquisition simultaneously via several parallel branches, performing express analysis in real time, and also combining electronics in the CAMAC, VME, and FASTBUS standards. The fundamental element of the DAQ system is a central VME crate (see Fig. 9), which contains the following elements: a VME crate system controller (SC); a CAMAC branch driver (BD); a controllable single-chip computer with integral MC68020 microprocessor (SCC); an interface (INT1) with a microcomputer, which served as the basis during the early stages of construction of the setup; buffer memory (M); and an interface (INT2) with personal computer like an IBM AT486, which controls the operation of the system, represents the information graphically, and sends the information to a storage archive.

An example of a DAQ system based on a VME crate is the VALET-Plus system at CERN. It consists of two processor subsystems.[43] On one side the system is connected to the instrumentation of the physical setup, and on the other it is connected to a personal computer that acts as a local peripheral server and provides a user interface. The VME crate contains commercially manufactured processor modules, EPROM, DRAM, a CAMAC branch driver, a graphics controller, and also interfaces with a FASTBUS highway, ETHERNET network, a GPIB device channel, and a SCSI interface.

The perfection of the VME standard has now been completed.[44] It is designed to be used for 64-bit data addressing and transfer simultaneously via address and data lines. New modules can operate on the same VME crate highway together with old ones.

3.1.3. Standards supplementing the VME standard

The VSB standard is designed for organizing local subsystems within a single VME crate highway. The VSB standard ensures that a processor module has access to memory and i/o sources via a separate local 32-bit bus not connected to the main highway, which considerably increases the throughput of interprocessor communications. There is a specialized adapter of the VSB bus, which ensures VSB signal transfer in the form of differential signals. This bus is called the VDB. It can transfer 32-bit data a distance of up to 5 m at a rate of 2 Mbyte/sec and a distance of 50 m at a rate of 1.2 Mbyte/sec. Any single-chip processor in the VME standard having an output to the VSB can be used as the control module of the VDB bus (see Fig. 10).[45]

The VIC standard is designed for organizing multicrate VME systems.[46,47] Signals propagate along a hanging cable highway consisting of two cables. The length of the highway can reach 100 m. The standard ensures the effective arbitration of several control modules, synchronous and asynchronous data-transfer protocols, simultaneous access to many devices, a simple mechanism for generating and processing interrupt signals, and high stability of failure.

3.1.4. The VXI standard

The VXI standard is an extension of the VME standard[48] and is designed for the construction of control–measurement

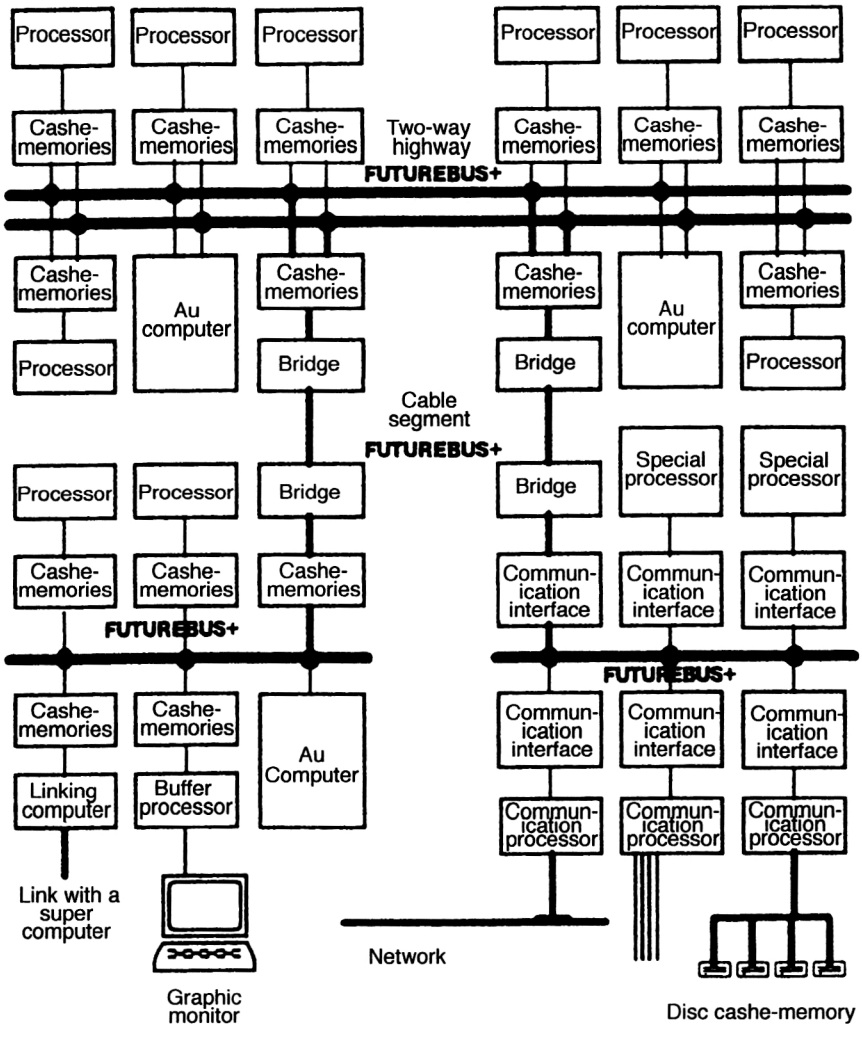

FIG. 11. Example of the architecture of a multiprocessor system using several FUTUREBUS+ highways.

devices. It combines the advantages of the high-performance VME highway with special features needed in the construction of high-current, noise-stable measurement devices: a power supply (± 24 W, ± 12 W, $+5$ W, -5.2 W, and -2 W), screening components, and special lines for transfer and summation of analog signals. The chip size can be 366.7×340 mm, which is significantly larger than the VME chip. The standard allows the design of recording-electronics modules for nuclear physics applications with characteristics comparable to those of modules constructed in the NIM and CAMAC standards (a high resolution of more than 14 bits and integral and differential nonlinearity of better than 0.1%).

3.1.5. High-speed open bus systems

FUTUREBUS+. The open standard FUTUREBUS+ defines the rules for constructing an expandable open bus system designed for 32-, 64-, 128- or 256-bit data transfer.[49] The design of FUTUREBUS+ depends on significant improvement of the performance and broadening of the functional possibilities of multiprocessor systems. The standard ensures complete independence from the architecture of the system and the type of processors used, and the use of both the basic asynchronous data-transfer protocol (up to 900 Mbyte/sec) and an auxiliary protocol with source synchronization, which allows the maximum possible data transfer rate (up to 2 Gbyte/sec) and permits instantaneous control over each block of transferred data. The use of fully distributed arbitration protocols and parallel operations decreases the number of mechanisms through which error can arise. Parity protection and feedback control are introduced wherever possible. For example, modules using the highway can write data into their own registers to perform self-control functions. The use of multilevel module-blocking mechanisms prevents hangup and blocking of the system. In Fig. 11 we give an example of the architecture of a system based on several FUTUREBUS+ highways.[49] To achieve maximum performance, the processors, the specialized processor, the i/o processors, the buffer processor of the graphics monitor, and the connection bridges are connected to the highway only via individual cache-memories or special communications interfaces.

SCI. The SCI standard determines the construction of an expandable multiprocessor system with up to 64000 nodes using a design based on very simple node–node connections. The rate of data transfer between nodes reaches 1000 Mbyte/

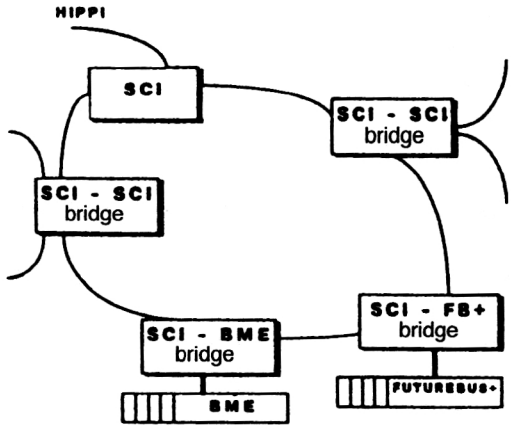

FIG. 12. Combination of electronics in various standards using the SCI standard.

sec. At present, there is a working model which ensures a rate of 500 Mbyte/sec (Ref. 50). The maximum transfer rate is achieved for the transfer of 16-bit code over short distances not exceeding several meters. The use of optical cable ensures bit-by-bit transfer over distances of up to 2 km, and the use of coaxial electrical cable ensures transfer over distances of up to several tens of meters at a rate of 125 Mbyte/sec. A node can be a processor, memory, i/o device, or bridge module ensuring passage from one bus to another. The standard supports the coherent operation of memory caches distributed throughout the system. In Fig. 12 we give an example of the architecture of an imbeddable system which combines several subsystems realized in various standards.[51] In Fig. 13 we show the basic elements of a modern DAQ system which can be constructed on the basis of the SCI standard[50] ensuring fast communications:

- Organization of access to many data buffers (DPM—dual-port memory), to which information, after appropriate filtering, is sent from the recording-electronics modules.
- Organization of high-speed information transfer over sizeable distances via optical lines connecting electronics modules located directly at the detectors, and hardware control of the experiment.
- Organization of $\mathbf{n}\times\mathbf{m}$ switchings of n event fragments to $\mathbf{m}$ event-acquisition processors.

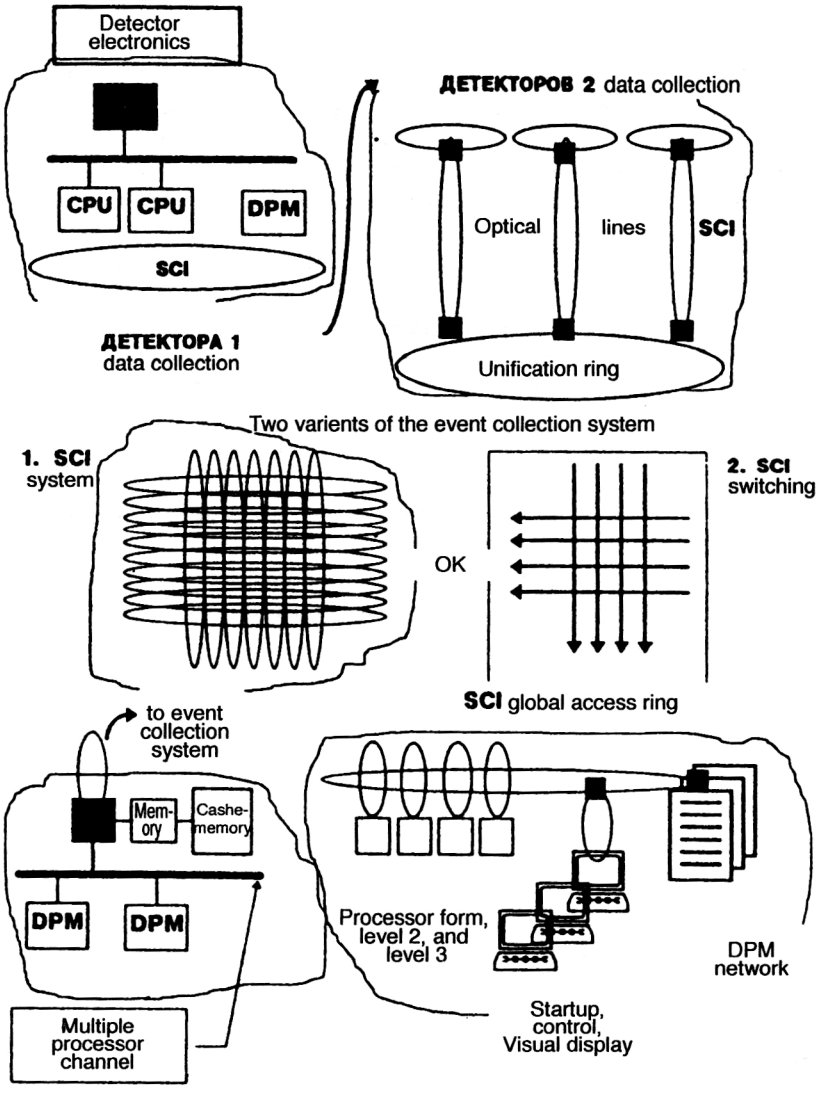

FIG. 13. Example of the use of an SCI highway in the construction of a DAQ system.

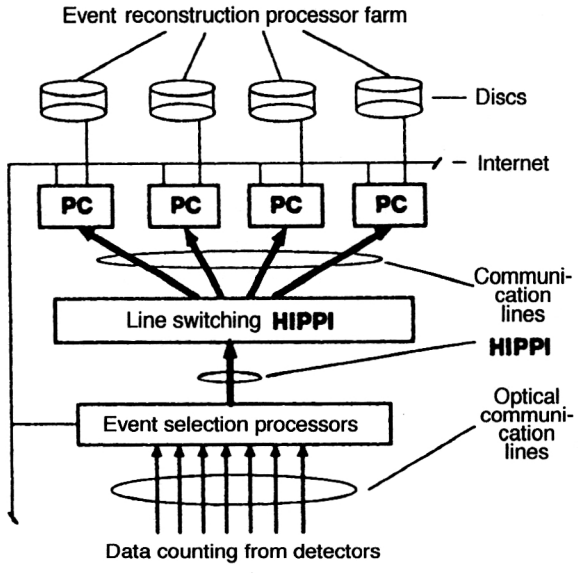

FIG. 14. Example of the use of the HIPPI standard in the NA48 setup.

• Organization of an interface with a processor farm performing the level-3 event selection.

• Links to work stations and long-term data-storage devices.

HIPPI: The HIPPI (High Performance Parallel Interface) standard defines an efficient protocol for one-way data transfer at rates of up to 100 or 200 Mbyte/sec for object–object connections.[52,53] A single cable of 50 twisted pairs is needed to reach a rate of 100 Mbyte/sec, and two cables are needed to reach 200 Mbyte/sec over distances of up to 25 m. The use of optical cable allows longer (up to 10 km) bit-by-bit data transfer at rates of up to 1200 Mbaud. Two HIPPI channels are used for two-way data transfer. The HIPPI standard is the ideal communications method for modern DAQ systems, which require transfers of up to several tens of Mbytes of data per second. One example where this problem is solved is NA48 at CERN (see Fig. 14).[54] This setup records up to 100 Mbytes of data per spill (2.5 sec) every 15 sec. These data are transferred to a processor farm (work stations) for level-3 event selection. The hardware realized in the HIPPI standard solves a fundamental problem in the experimental setup: the problem of the high-speed transfer and distribution of a large amount of experimental data among the processors of the event-building farm.

Fiber Channel: The Fiber Channel (FC) standard was originally developed for high-performance communications with switching and two-way data transfer, which ensures the high-speed exchange of large blocks of data between processors and peripheral devices. The limits of the standard were later extended to make it usable for switching data packets in a network. The FC provides data transfer at rates from 132.812 Mbaud to 1.0625 Gbaud via a series coupling line.[55] Signal transfer can be done using a single optical line, several optical lines, a twisted pair of wires, or a coaxial cable.

ATM. The ATM standard defines a mechanism for switching data flows.[56] It ensures data transfer at rates from 100 to 622 Mbyte/sec. This standard is most useful for creating networks.[57]

3.2. Processor elements in DAQ systems

The ever-increasing speed and packing density of microelectronic devices is constantly and strongly influencing the evolution of the architecture of computational devices (computers, work stations, the single-chip processors of open bus systems). In Fig. 15 we show the trends in the increase of the speed and packing density of semiconductor elements.[58] The appearance of microprocessors had the strongest effect on the architecture of DAQ systems.

3.2.1. Microprocessors

At present, there are a great many different microprocessors. We shall consider those which are used most often in the electronics for experimental setups in high-energy physics and relativistic nuclear physics. Among the simplest and least expensive microprocessors are microcontrollers, and among the most complex are RISC and CISC general-purpose processors, specialized transputers, and DSP processors.

A **microcontroller** contains all the elements needed for constructing a complete computer. It is designed for use in various programmable control systems.[59] A microcontroller has an extended set of sequentially executable commands, and it operates with 4-, 8-, or 16-bit data words. As a rule, it performs operations over several processor cycles, and only on fixed-point variables. It operates with low performance, small energy requirements, and its cost is low.

A **transputer**, a type of microprocessor, is designed for the construction of computing systems with operations executed in parallel.[59] Four embedded high-speed coupling lines are responsible for the inter-processor communications

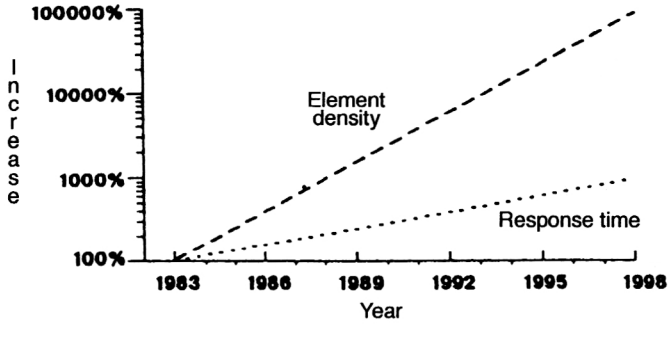

FIG. 15. Increase of the speed and packing density of semiconductor elements.

and make it fairly simple to construct highly efficient parallel systems. The synchronization of i/o operations via the coupling lines is automatic. Operations are performed on 32-bit data. The transputer performs operations sequentially over several processor cycles. Both fixed- and floating-point variables are used. One of the most recent transputer models is the T9000 made by INMOS. It has a peak performance of 200 million operations per second or 25 megaflops and ensures data transfer over a single coupling line at a rate of up to 100 Mbyte/sec.[60]

RISC microprocessors are designed for use in high-performance computers and provide maximum efficiency because they perform only a restricted set of operations.[61] From one to several operations on 32- and 64-bit words can be performed in a cycle. Most of the modern RISC processors can perform floating-point operations in a single cycle. The processor is designed to work with high-speed registers, the number of which can reach 32 and more, and with cache-memory. All operations except data input and output from RAM are performed on operands contained in the registers. It should also be noted that RISC processors operate with maximum efficiency only when optimized compilers are used.

DSP is a specialized microprocessor designed for optimal signal processing.[59] DSPs use an intensive conveyer mode, and hardware rather than software control. They can operate with several independent memories with a large address space. They contain functional nodes working in parallel. The construction of a series of DSPs is in most cases optimized for executing certain algorithms (a digital filter) or specialized applications (modem connections, acoustic analyzers/synthesizers). The new DSP to be produced by Texas Instruments, the TMS320C54x, will perform at a level of 100 million operations per second.[62]

CISC microprocessors are involve many very complicated technical solutions and contain a large set of highly complex commands.[59] The commands can manipulate bits, bytes, words, and longwords in both fixed- and floating-point form. The interface provides simple and at the same time efficient communications with a bus for the transfer of data of various widths (8, 16, and 32 bits). The architecture of the processor allows it to operate in multitask and multiprocessor modes.

Embedded controllers (Motorola MC683XX, Intel 80960) are characterized by a high degree of integration, high performance, and low energy requirements. They are designed to be embedded in various control devices used to control processes, robotics, instrument manufacture, aviation, and so on.[59] Such applications require that the time for processing interrupt signals be small. Microcontrollers operate using 32-bit fixed- and floating-point data. The construction of the processor can involve circuitry for controlling direct memory access channels, an analog-to-digital transformer, a timer, and other components needed for specific embedded applications.

3.2.2. Processor farms

Among the most remarkable applications of processors used in DAQ systems are processor farms (PFs). A PF is a set of processing devices of the same type connected to each other for performing a single calculation in parallel on a set of events. PFs were initially designed only for the final analysis of data already stored in archives. Later they became widely used as components of DAQ systems for final event filtering.

The first PF used 3081/E emulators.[63] The 3081/E emulates the command set of computers of the IBM 370 series. The performance of the emulator is as good as that of the IBM 370/168, and it costs much less. A flexible high-speed interface allows the creation of a PF consisting of several 3081/E devices (DELPHI, L3).

The PF (CDF) built by the ACP project has found extensive application.[64] It consists of a set of single-chip VME processors (MC68020). The VME crates are connected via a specialized fast highway (20 Mbyte/sec).

The ZEUS setup uses a PF whose elements are Silicon Graphics work stations (SGI). Thirty SGI are distributed among 6 VME crates and are connected by a fast ACP highway.

4. THE ARCHITECTURE OF MODERN DAQ SYSTEMS

In this section we discuss examples of microprocessor DAQ systems operating at accelerators with colliding beams (colliders): LEP at CERN, HERA in Hamburg, the Tevatron at Fermilab, and also the systems designed for experiments at RHIC in Brookhaven and LHC at CERN. The architecture of these DAQ systems reflects the most important trends in the development of techniques for constructing real-time multiparameter multiprocessor systems used in experiments in high-energy and relativistic nuclear physics. The setups that we discuss contain an enormous number of recording channels and control points, and impose extreme requirements on the technical characteristics of the electronics, the throughput of the coupling lines, and the performance of the processor elements.

In Table I we compare the characteristics of accelerator-colliders and give estimates of the number of interactions per beam intersection and the fraction of events selected.

Information on the number of recording channels and the event recording rate for these setups is given in Fig. 16 (see Refs. 65 and 66).

4.1. LEP accelerator

The LEP accelerator was designed to accelerate electrons and positrons to an energy of 55 GeV during the first stage of its development, and to 95 GeV in its second stage.[67,68]

At the LEP accelerator there are four experimental setups: ALEPH, DELPHI, L3, and OPAL. Each of these records interaction products in a solid angle of 4π and identifies the elementary particles. Each setup contains nearly the same set of devices necessary and sufficient for the construction of the detector system: solenoidal magnets, a central track chamber, electromagnetic and hadronic calorimeters, a muon detector, and a luminosity-monitoring system.

The creation of these four setups at LEP marked the beginning of a new stage in the development of DAQ systems. Each setup contains a multilevel event-selection sys-

TABLE I.

	LEP, CERN	SppS, CERN	HERA, Hamburg	Tevatron, Fermilab	RHIC, BNL	LHC, CERN
Particle beams	e^+-e^-	$p-p^-$	e^--p	$p-p^-$	from $p-p$ to Au–Au	$p-p$
Intersection period	22 μs	3.8 μs	96 ns	3.5 μs	112 ns	25 ns
Luminosity, $cm^{-2}\,s^{-1}$	3×10^{34}	10^{31}	2×10^{31}	10^{30}	$p-p$ 2×10^{33} Au–Au 2×10^{26}	$1-5\times10^{34}$
Number of interactions per intersection	$\ll1$	≈1	$\ll1$	$\ll1$	$p-p$ 0.2 Au–Au $\ll1$	≈20
Percent of selected interactions	100	0.1	100	100	100	0.001

tem with a large number of processors at all levels. The multilevel event-trigger systems reduce the rate of event acquisition to 1 or 2 events per second when level-1 trigger signals appear with a frequency of about 45 kHz. Most of the components of the DAQ systems are constructed in the CAMAC, FASTBUS, and VME standards, which solves the problems of **volume**, organization of the needed **communications**, and distribution of **processors** over levels. Data on the use of devices[69] in these standards for all four setups are given in Table II.

4.1.1. DELPHI

Scientists from the JINR are taking an active role in the construction and implementation of the DELPHI setup. The data acquisition and experimental control functions are distributed among 19 autonomous subsystems.[70] This ensures a high degree of independence of the data acquisition subsystems in each of the 16 detectors of the setup. The trigger and global data acquisition systems are treated as separate subsystems. Twenty VAX computers are responsible for the control and monitoring functions in the DAQ systems. In designing the DAQ systems, special efforts were made to limit the diversity in the types of electronic device used. The recording electronics were realized in the FASTBUS standard. Subsystems were assigned the task of exerting slow control over the technical parameters of the detector (the gas, voltage, pressure, temperature, and so on).

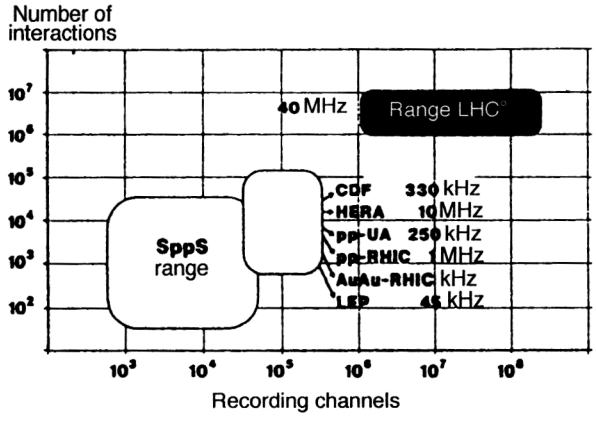

FIG. 16. Graph of the ratio of the number of data channels and the rate of recording events in current experimental setups.

In Fig. 17 we show the instrumentation contained in the DELPHI DAQ system, which has a multilevel tree structure. Each subsystem in the autonomous mode performs a complete and independent acquisition of data, detector calibration, and instrument monitoring without interacting with the other subsystems. The quality of the information obtained is monitored during the data acquisition by each detector. The subsystems are controlled by 13 μVAX-11 computers, which are connected to the FASTBUS apparatus via single-chip CFI processors. The main elements ensuring data acquisition in the system are 70 single-chip processors in the FASTBUS standard (FIPs). Of these, 52 processors act as crate processors (CP), 11 act as processors which assemble event fragments (LES), 6 perform both these functions simultaneously, and one acts as a processor which assembles the complete event (GES).

Each level of the DAQ system forms a unit cell.[71] All the cells have identical structure. Each contains two sets of buffers (input and output), and also elements which regulate transfer and control processes. The main task of a cell is to transfer data from the input to the output buffer. A cell is triggered by the cell above it, and it in turn triggers the next cell. Data transformation and processing can occur in each cell. The DELPHI DAQ system contains a base of six levels of cells in each branch. In the **recording cell** the data from the detectors are transformed into digital code. The output buffer (FEB) is designed to accept four events. The FEB is filled by real trigger signals from an event (see Fig. 18). In the FASTBUS **crate cell** the processor CP sends data from the FEB to its buffer CEB. The **subsystem cell** consists of a set of crates and serves a detector or part of a detector; for example, the chamber TPC is served by two subsystems. The LES processor sends data from the CEB buffers to the event-fragment buffer (MEB) and the buffer SEB (see Fig. 18). The two buffers are designed to contain 256 events. The SEB

TABLE II.

Bus	Number of IC per module	Number of modules per crate	Total number of modules used in a crate	Cost per IC (US $)
CAMAC	80	25	12000	8.28
VME	100	21	12600	6.62
FASTBUS	300	26	23400	4.14

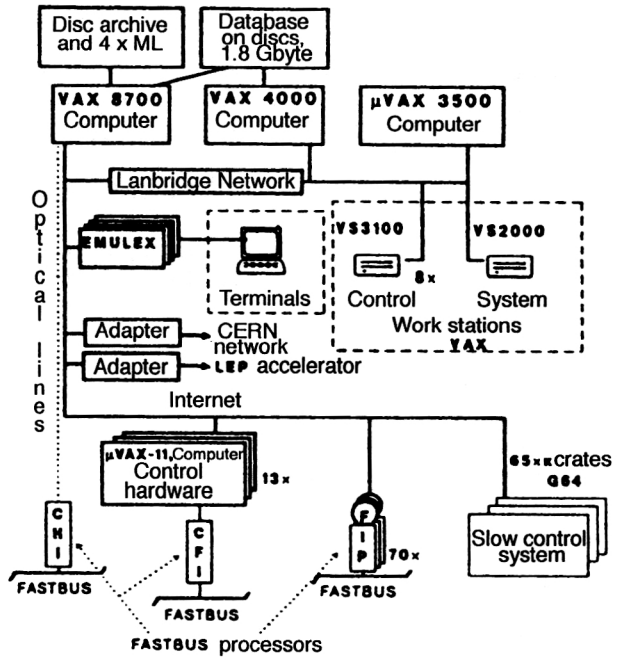

FIG. 17. The complex of computing elements in the DAQ system of DELPHI.

is needed to organize autonomous operation with a single detector. When the data acquisition is complete, it is used to monitor the working detector. In the **central subsystem** two processors participate in the transfer of data from the MEB buffers to the complete-event buffer (GEB). The actual data transfer is performed by a fast controlling FASTBUS module (BM). The GES processor controls the data transfer and assembles the complete event (see Fig. 18). The complete event is sent from the GEB to the processor farm consisting of **3081/E emulators**[63] for preliminary data processing (Fig. 18). The data are sent to a central VAX for **storage.**

VS3100 work stations provide a user interface to the system and graphical representation of the events and histograms for groups of detectors. VS2000 work stations are used as servers for the embedded processors, data-base servers, documentation processors, and so on.

4.1.2. ALEPH

The block diagram of the DAQ system of the ALEPH setup[72] is shown in Fig. 19. Devices in the FASTBUS standard are also used for this system. The largest detector in the setup is a large time-projection chamber (TPC), the data from which flow through nearly 50000 data channels. The

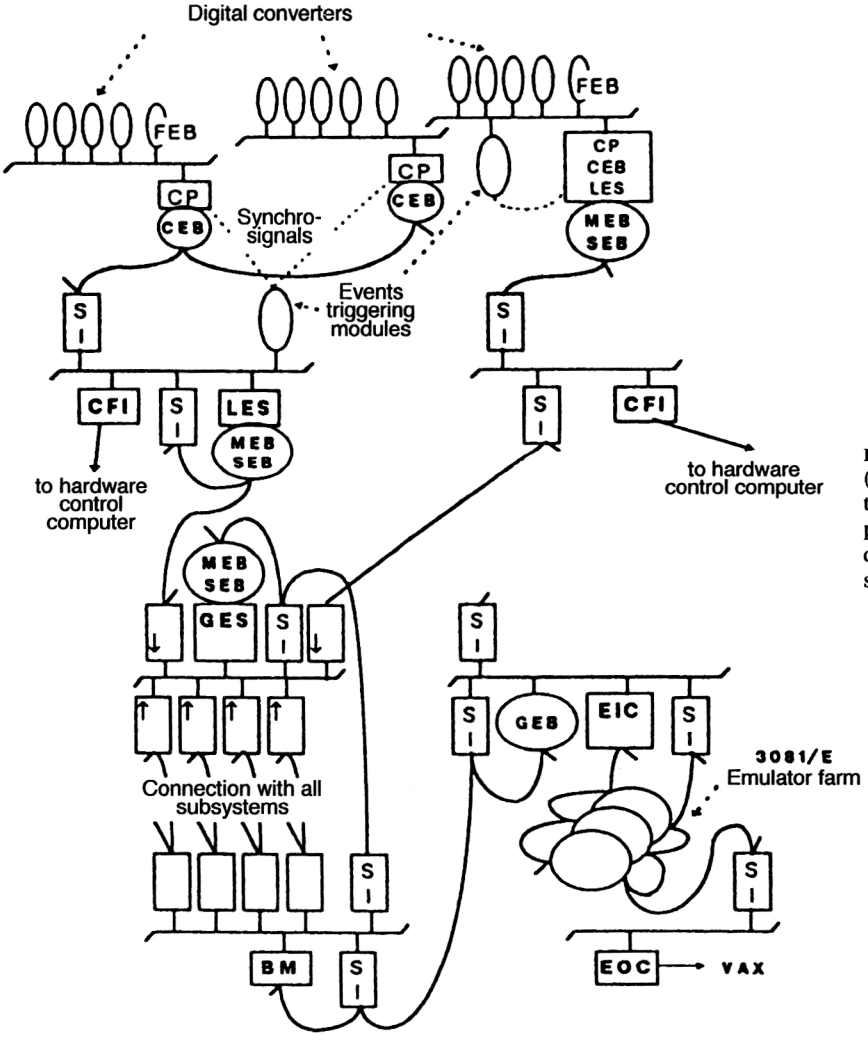

FIG. 18. Block diagram of two data readout subsystems (in the first the CP and LES functions are divided between two FIP processors, and in the second they are performed by a single FIP), and of the central data acquisition subsystem in the DAQ system of the DELPHI setup.

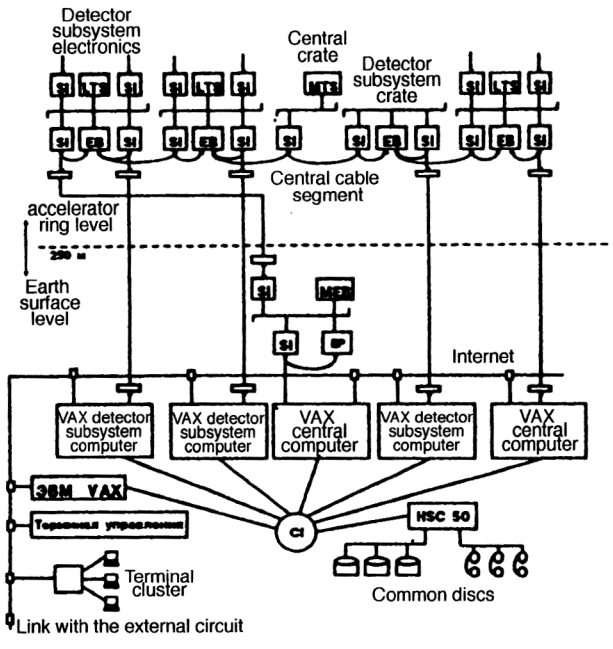

FIG. 19. Block diagram of the DAQ system of the ALEPH experiment.

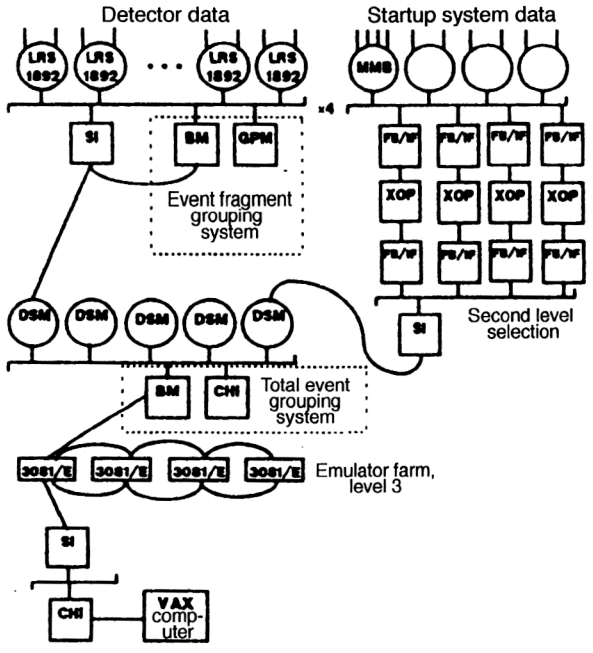

FIG. 20. Block diagram of the DAQ system of the L3 setup.

system for recording data from the TPC occupies 110 FASTBUS crates. About 250 FASTBUS crates are involved in the entire DAQ system.

Each detector has its own data acquisition subsystem, whose control link is a FASTBUS crate containing an event-fragment assembly module (EB) and a local synchronization module (LTS). The EB module reads out information from the detector via the synchronization signals and then sends it to memory designed to store several event fragments. A VAX computer is connected to each subsystem and uses the information obtained to monitor the operation of the subsystem. The MEB module assembles the complete event under the control of the main synchronization module MTS. The complete event is analyzed in real time by a special processor EP.

4.1.3. L3 setup

L3 is the largest of the four setups. In the DAQ system there are 4 parallel data streams coming from the main detectors, and a separate data stream for processing trigger signals of the three-level event-selection system.[73] The DAQ system is almost completely based on electronics in the FASTBUS standard. In Fig. 20 we show the block diagram of the DAQ system of the L3 setup. Data from the recording electronics of the detector flow into LeCroy 1892 memory modules at a rate of 16 Mbyte/sec. The data on an event fragment from each detector are then collected in a two-input memory (DSM). The use of a special module (BM) for transferring blocks of data ensures a very high rate of data transfer between memories. The processor GPM based on an MC68000 microprocessor controls the operation of BM and formats the transmitted data. The BM and GPM assemble the event fragments from each detector, and the BM and the CHI, based on the MC68030 microprocessor, assemble the complete event. Level-2 event selection is performed by XOP processors specially constructed for high-speed calculations in level-2 selection.[74] To maintain the high rate of exchange (40 Mbyte/sec for input and 20 Mbyte/sec for output), external devices perform signal exchange via the standard LeCroy ECLine. A processor farm of 3081/E emulators is used for the level-3 selection. A processor of the CHI type is used to connect the FASTBUS system to the controlling computer.

4.1.4. OPAL

Altogether, this setup records 150 000 analog signals from 12 different detectors. There are three levels of event selection in the DAQ system.[75] The input data stream at nominal luminosity is 200 Kbyte/sec. Both standard (CAMAC and FASTBUS) and specialized modules are used to record information from the detectors. Scanning monitors in the CAMAC or VME standards read out information from the recording devices, store it, subtract pedestals, determine the location of clusters, suppress the unimportant part, and compress it.

In Fig. 21 we show the block diagram of the DAQ system of the OPAL setup.[76] Each detector is connected to its own data-acquisition subsystem. The central component of each is a local system crate in the VME standard containing a standard single-chip processor (FIC 8230), an 8-Mbyte memory module (DPM 8241), an ETHERNET interface (FILTABYTE 25.1), a local trigger module, and a series of modules which serve the detector. Most of the detectors have two local system crates which are located on opposite sides of the detector and which, are classified as main and auxiliary. The main crate is connected to the hardware which assembles the complete event.

The DAQ system of the OPAL detector uses a large number of devices in the VME, VSB, and VIC standards. In Fig. 22 we show the subsystem which performs readout from

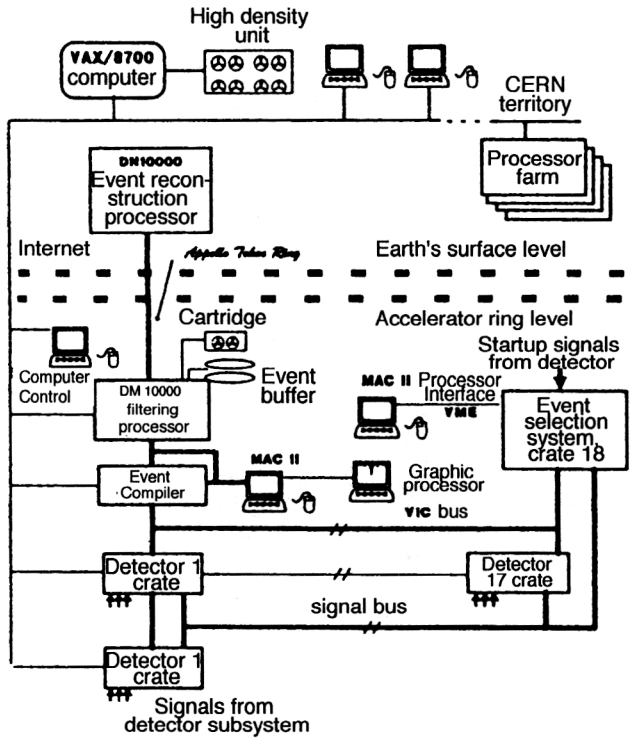

FIG. 21. Block diagram of the DAQ system of the OPAL setup.

the drift chamber. The data recording in the subsystem is performed by fast 96-channel ADCs (FADCs) located in 80 crates. Data readout from the ADCs, data compression on the basis of pulse-shape analysis, and also track reconstruction are performed by 22 processors in 2 VME crates: SP, a control processor; MP, a monitoring processor; and 20 recording processors (FP). A VIC bus connects the VME crates and creates a single address space in the subsystem. A Motorola MVME165 module is used as the single-chip processor.

In Fig. 23 we show the block diagram of the complex needed to assemble a complete event. The 18 separate subsystems are split into four groups, inside each of which the subsystems are connected by a VIC bus. The processor SP controls the event assembly and transfers the event to the

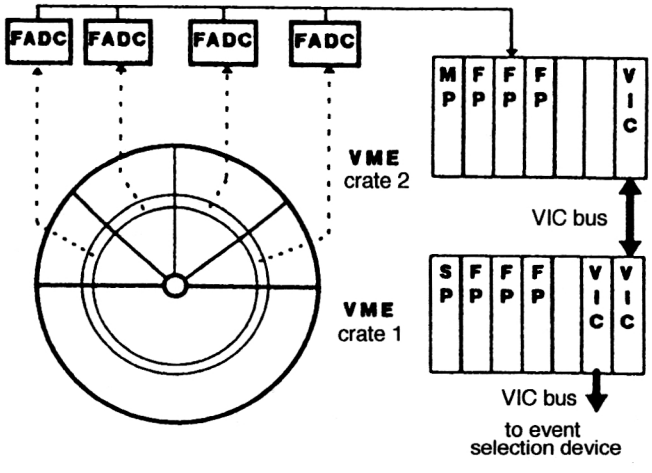

FIG. 22. Subsystem for data acquisition from a drift chamber.

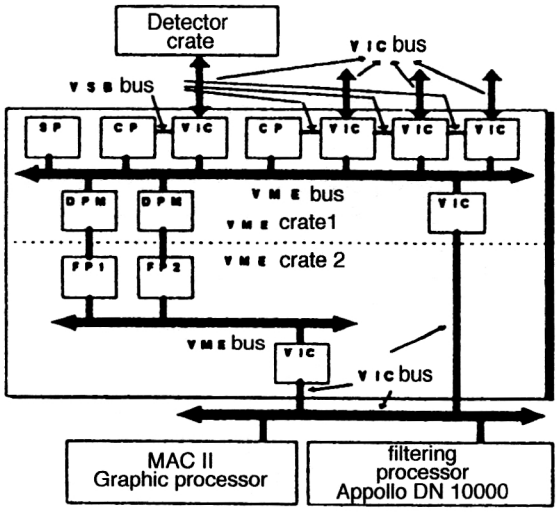

FIG. 23. Block diagram of the hardware complex needed for assembly of a complete event.

Appollo processor for level-3 event selection. The processors CP for moving blocks of data to 16-Mbyte, two-input memories (DPM) use direct-access channels. The processors FP1 and FP2 assemble the complete event on the basis of the information obtained from the subsystems.

4.2. The Tevatron

The Tevatron is a proton–antiproton colliding beam accelerator with center-of-mass energy 1.8 TeV. There are two experimental setups, CDF and D0, operating at the Tevatron. The experiments performed using CDF and D0 led to the discovery of the long-awaited top quark in 1994.[77]

4.2.1. The CDF setup

CDF is a 4π spectrometer.[78] Its DAQ system has about 100 000 data channels. The event-trigger system is based on the detection of clusters with energy release in calorimeters.[79] The selection coefficient is $10^3 - 10^4$.

In Fig. 24 we show a simplified block diagram of the DAQ system of CDF.[80] The part of the DAQ system pertaining to the devices which record data from the detectors uses a specially designed analog system RABBIT. The digital part of the DAQ system consists of modules in the FASTBUS and VME standards. Altogether, the system contains 53 FASTBUS crates. Special high-speed scanning processors send data transformed into digital code from the RABBIT system to the FASTBUS modules. Level-3 event selection is performed by a processor farm of the ACP type made of 50 single-chip processors.[64] Each processor has a 6-Mbyte RAM. A cluster of VAX computers is used to monitor the acquired data and also to calibrate the detectors and perform diagnostics of the functioning of the hardware.

4.2.2. The D0 setup

The D0 setup consists of seven main detector subsystems and has about 115 000 recording channels. The recording electronics send events 300 Kbytes in length at a rate of from 200 to 400 GHz.

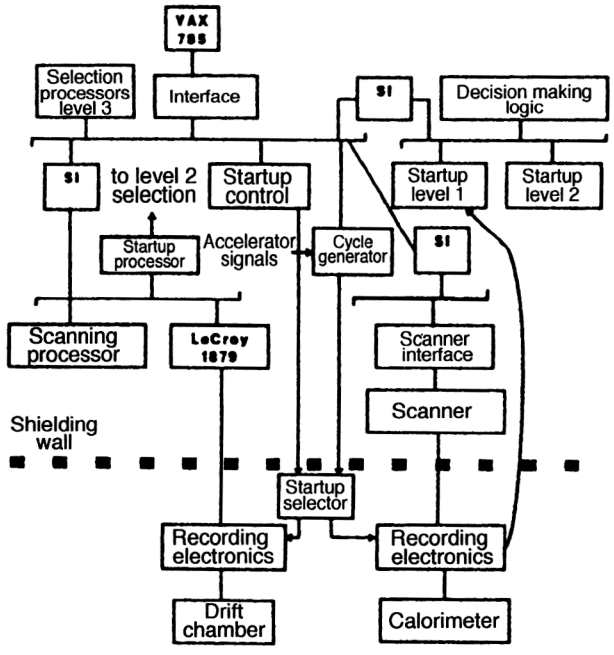

FIG. 24. Simplified block diagram of the DAQ system for CDF.

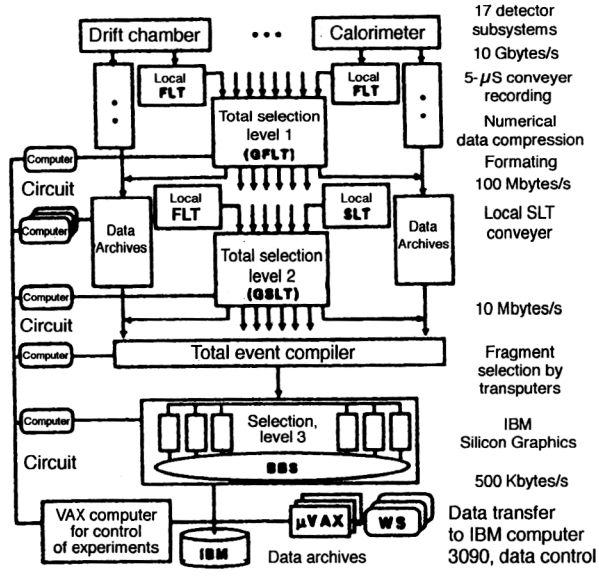

FIG. 26. Block diagram of the DAQ system for the ZEUS experiment.

The DAQ system is based on devices in the VME standard (see Fig. 25).[81] The structure of the DAQ system is fairly simple. Analog data are transformed into digital code in 89 VME crates divided into seven groups according to the type of detector. The data from each group of crates and from the level-1 selection device are then sent at a rate of 40 Mbyte/sec via eight 32-bit one-way lines to a processor farm containing 50 microVAX computers for performing the event selection (filtering).[82,83] After this procedure, events are transferred at a rate of 2 Hz to an archive for long-term storage. The use of one-way lines simplifies the design of the fast data acquisition, but requires the introduction of additional communications for transferring information about pedestals and other parameters. This feedback occurs via the lines of the system which controls and monitors the operation of the setup hardware.

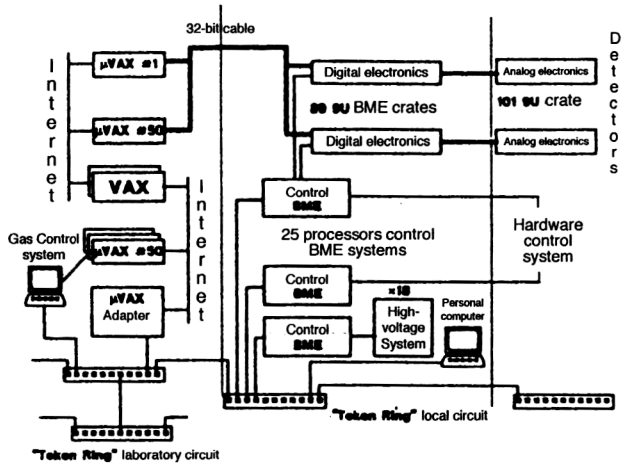

FIG. 25. Architecture of the DAQ system of the D0 setup.

4.3. The HERA accelerator

HERA is a proton–electron colliding beam accelerator. The protons are accelerated to 820 GeV, and the electrons to 30 GeV.

At this accelerator there are two multipurpose experimental setups[84] for recording the products of *ep* interactions in nearly the entire solid angle (4π): ZEUS and H1. In addition, the construction of the HERA-B setup[85] is nearly complete, and it should begin operation in 1998. The JINR is also involved in the creation of HERA-B.

The detectors of these setups can generate up to 3 megabytes of primary information per event. The present methods of data acquisition can handle only several hundred kilobytes per second, and so in the acquisition process it is necessary to compress, format, and filter the data to the desired event size and writing rate. A multilevel event-selection system ensures a data acquisition rate of about five events per second after the final filtering. Each setup uses a specialized conveyer trigger system, which ensures preliminary selection of event candidates at a background level of 10^4.

4.3.1. The ZEUS setup

ZEUS consists of a large number of different types of multichannel detector and has 270 000 data channels.

A block diagram of the DAQ system is shown in Fig. 26 (Ref. 86). It involves 17 detector subsystems, each with its own system for conveyer data readout and event selection up to the device which assembles the complete event (EVB). The level-4 selection allows the information flow to be decreased from 3 Tbyte/sec to 0.5 Mbyte/sec.

At level 1 the local (FLT) and complete (GFLT) event-selection devices use specialized high-speed hardware which digitizes, compresses, and packs the data.[87]

At level 2 the local (SLT) and complete (GSLT) selection devices perform an analysis using the digitized data. Transputers are used to make decisions in many SLTs. VME

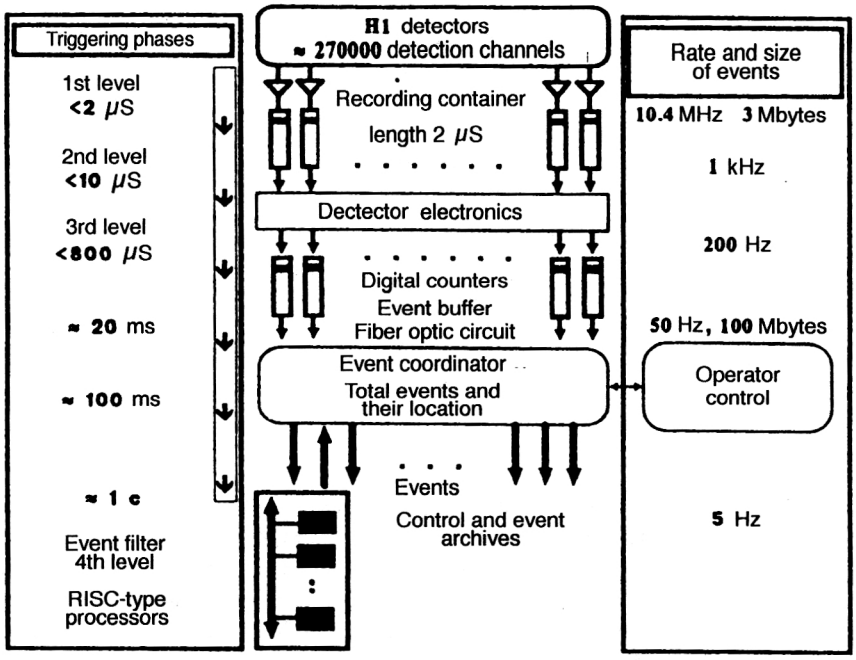

FIG. 27. Architecture of the DAQ system for the H1 setup.

transputer modules like the NIKHEF 2TP are used to couple the SLT to the GSLT, ensuring a transfer rate of 20 Mbyte/sec.

A farm of Silicon Graphics UNIX work stations is used for the level-3 selection (TLT). The total performance is 1000 million operations per second. Thirty Silicon Graphics work stations are distributed among 6 VME crates, which are connected by a high-speed bus (BBS) developed by the ACP project at Fermilab.[64] Data are sent to the TLT from the device which assembles the complete event (EVB), which consists of a programmable 64×64 switch of multibit lines (64 input and 64 output) and VME transputer modules of the 2TP type. The EVB can contain up to 76 complete events.

After the level-3 selection the events are written on magnetic tapes with very high information density. Some of the events are sent to a cluster of 15 microVAX computers for instantaneous monitoring and visualization and can be accessed by experimentalists using work stations (WS). This cluster is connected via an Ethernet link to 20 peripheral processors, which in the autonomous mode provide local monitoring and control over nearly every element of the system, and also prepare and load the needed programs and constants into all the processors.

Single-chip VME processors are used to monitor the operation of the high-voltage sources, the gas instrumentation, the temperature, and other parameters which vary slowly in time. Thus, VME is the basic standard used in the construction of the DAQ system for ZEUS.

All the processor elements of the DAQ system are connected to form a local network, which corresponds to a new concept in the architecture of DAQ systems for experimental setups.

4.3.2. The H1 setup

In Fig. 27 we show the structure of the DAQ system for H1 (Ref. 88). In H1 the event transmission rate after the level-1 trigger theoretically should be less than 10 kHz (at the time of exposure to the beam this value is about 100 Hz), in order for the level-2 selection processors to have about 10 μsec to perform the needed analysis and output the go-ahead for data readout from the recording electronics.[89]

4.3.3. The HERA-B setup

The DAQ system of HERA-B is characterized by a very complex four-level event-selection system (the selection coefficient is 10^6; Ref. 85). Each of the selection systems at levels 2 (L2), 3 (L3), and 4 (L4) is a processor farm. The decision time in L1 (track reconstruction) is 10 μsec, in L2 (tracks in magnets, vertex reconstruction) it is 10–50 μsec, in L3 (particle identification) it is 100 μsec, and in L4 (complete reconstruction of the event) it is 4 sec. L2 and L3 are identical in construction, each containing 10 processor elements and operating in real time. They must be connected to a data buffer via a high-speed network (40 Mbyte/sec). Personal computers will probably be used as processors. L4 is separate from the main part of the DAQ system and should contain up to 200 processors connected to a Fast-Ethernet network. Variants where the Power PC 604e/200 MHz or the Pentium Pro/200 MHz are used as the processor elements are being considered.

4.4. The LHC accelerator

The LHC accelerator is under construction. It will be a large accelerator–storage-ring complex using colliding proton beams, each of energy 7.7 TeV. It will be located in the tunnel of the LEP accelerator at CERN.

Three setups, ATLAS, CMS, and ALICE, are being built to perform experiments at LHC. The luminosity at LHC corresponds, on the average, to the appearance of up to 20 inelastic events per beam intersection (once every 25 nsec). Therefore, the events of interest, which correspond to rare

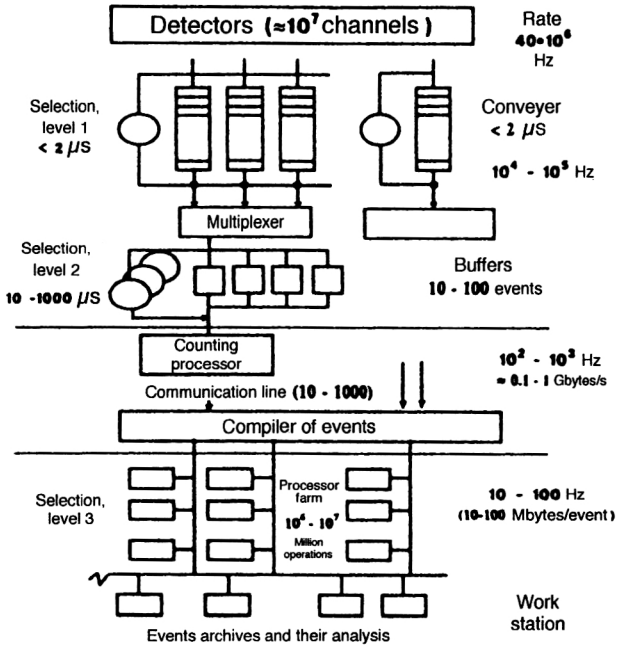

FIG. 28. Generalized block diagram of the DAQ systems for the LHC experiments.

physical processes, will be immersed in a background of particles from other insignificant events[90] amounting to 10^9 events/sec or, for 10^7 data channels, about 10^{15} bytes/sec.

Among the main features of the DAQ systems to be used at LHC are the following:

1. Decision time of the level-1 selection system exceeding 25 nsec (the time interval between beam intersections);

2. Memory of a detector cell also larger than 25 nsec (the maximum time to drift over 4 mm of detectors is 40 nsec);

3. Superposition of events and superposition of signals from the detectors;

4. A very large number of data channels.

The DAQ systems must be able to handle data arriving at very high rates, select the events most interesting from the viewpoint of the physical processes to be studied, and store these events for subsequent analysis. The system must be designed to reach the maximum performance by using a data conveyer at the level of the detector electronics, by transferring the data through the hierarchy of levels, and by parallel operation of individual elements of the system.

In Fig. 28 we show the block diagram of the generalized DAQ system for the experimental setups at LHC.[91] The level-1 selection system must ensure decrease of the input event stream from 40 MHz to 100 kHz. The selection is performed by specialized hardware based on fast analysis of signals from individual detectors.

One of the most complicated problems is the assembly of an event from the fragments arriving from different detectors. The event flow after the level-1 selection is ≈ 100 kHz, and the event builder must possess a throughput of about 100 Gbyte/sec distributed over many parallel channels. Preliminary estimates of the computing resources suggest that it will be necessary to use 1000 processors, each performing at a level of from 10^3 to 10^4 million operations per second.

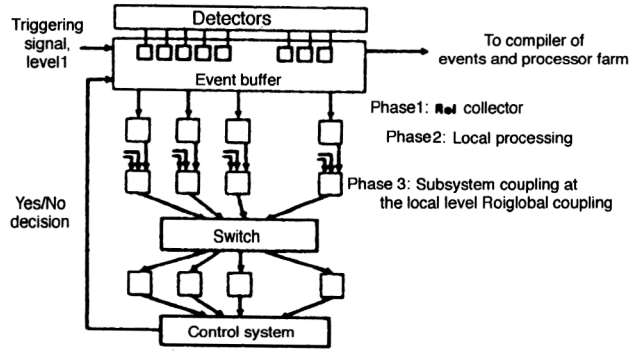

FIG. 29. Solution of the problem of event-stream filtering in the ATLAS experiment.

There are two approaches to solving the problem of filtering the event flow from 100 kHz to 100 Hz.

In the ATLAS experiment[92] (see Fig. 29) it is proposed that events be filtered in two stages, by dividing the selection system into a set of parallel and, as far as possible, conveyer operations and distributing the processing among several sets of processors. Only RoI (Regions of Interest) data fragments selected at level 1 will be used for the level-2 selection. They will be processed in parallel by sets of independent processors and processors which use the conveyer technique. Then the complete event will be sent to the level-3 selection system for a final decision.

In the CMS experiment (see Fig. 30) it is proposed that the event selection and assembly be split into only two stages: virtual level-2 selection and level-3 selection. The level-2 selection will be performed by the same processor farm which analyzes the complete event. The decision about the level-2 selection will be based on analysis of part of the data. If an event satisfies the selection criteria, the rest of the data on that event will be sent to the same processor for a final decision (level-3 selection), after which the information will be stored.

For the ALICE program[93] it is proposed that an experimental setup be designed to record nuclear–nuclear interaction products at the energies of the LHC colliding-beam accelerator. The setup will consist of several multichannel detection subsystems (see Fig. 31). The proposed size of an event is from 20 to 50 Mbytes. The DAQ system must satisfy very stringent requirements on performance and architecture. The rate of event aquisition in nuclear experiments is

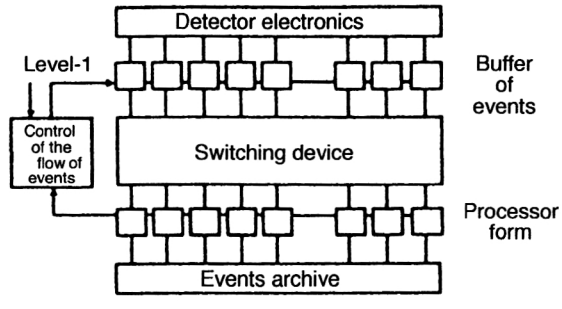

FIG. 30. Solution of the problem of event-stream filtering in the CMS experiment.

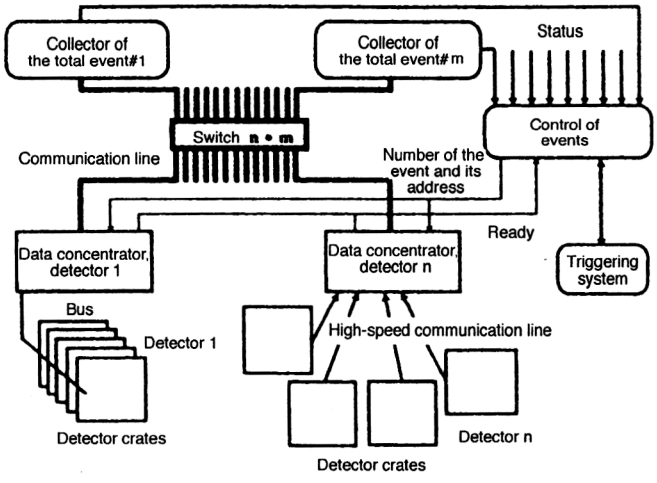

FIG. 31. Block diagram of the DAQ system being developed for ALICE.

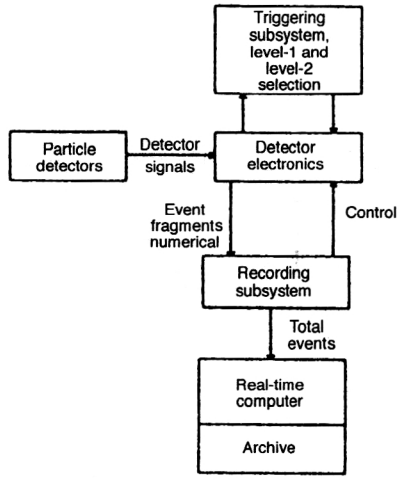

FIG. 32. Structure of the DAQ system of PHENIX (RHIC, Brookhaven).

lower than in pp experiments, but the event sizes are considerably larger, and so the requirements on the performance are comparable. Since an individual device cannot receive data arriving at a rate of several Gbyte/sec, it may not be possible for the DAQ system to have the classical branch structure. The data arriving from parallel branches of the recording electronics will be sent via a switching matrix to a set of devices which assemble the complete event. Here the throughput of the communications channels must be 100–200 Mbyte/sec. A large part of the recording electronics and digital transformers will be located directly at the detectors or near them. They will be connected to the DAQ system via digital busbars or optical lines. Versions using the VME-D64 ($\approx$80 Mbyte/sec) and FUTUREBUS+ (up to 200 Mbyte/sec) are being considered.

It is believed that a channel throughput of about 10 Mbyte/sec will be sufficient for the intercrate connections. This will be achieved using dedicated two-way optical communications channels (SCI, HIPPI, etc.). These channels will be connected to switching matrices. Even if it proves technically possible for a channel to allow the multiprocessor mode, it is proposed that only two-way communications be used, in order to (1) prevent collisions between information packets, (2) ensure a completely determined and minimum dead time per event, and thereby (3) decrease the requirements on the buffer memory. The latter will in any case amount to several tens of gigabytes.

4.5. The RHIC accelerator

The construction of the Relativistic Heavy Ion Collider, RHIC, should be completed in 1999 in Brookhaven National Laboratory.[66] It is designed to accelerate heavy ions to 100 GeV in each beam. It is expected that this energy will be sufficient for formation of the quark–gluon plasma. Experimental research will be carried out at this collider using two large multichannel spectrometers PHENIX and STAR, which will record the interaction products of the accelerated heavy ions. These detectors are not yet finished, and the features of their DAQ systems described here are not firmly established, since many elements of these systems are in the developmental stage.

The main goal of the experimental research at PHENIX[94] is the study of the properties of a new phase of matter: the quark–gluon plasma. Although this setup will focus on the detection of leptons (electrons and muons), it will also be capable of highly efficient hadron and photon detection.

The DAQ system of the PHENIX setup should allow data acquisition from about 200 000 detection channels. Its main subsystems are shown in Fig. 32. The electronics of each detector subsystem include buffer memory for conveying the recorded data, the arrival time of which will be synchronized with the beam intersections in the collider. These data will be marked, filtered in accordance with the decisions of the level-1 and 2 event-selection subsystems, transformed into digital code, compressed, and sent to the recording subsystem in the form of event fragments via $\sim$50 optical communications lines.

The recording subsystem consists of three parts: the recording electronics, the event builder, and a level-3 event-selection device. The architecture of the recording subsystem and its coupling to the synchronization system, the trigger system, the data-acquisition computer, and the slow-control subsystems are shown in Fig. 33. There are plans to use VME, FASTBUS, and specialized buses in the construction of the recording subsystem for organizing the individual components of the subsystem. The recording subsystem will be constructed using standard segments, including general-purpose communications media and four types of module: MCS, a control and calibration device; LTS, a device for processing local trigger signals; ROC, a device for controlling the data readout; and DCM, a data storage device. It is planned that the recording modules for each detector subsystem will occupy a single crate at 20 positions. From the detector electronics the data reach the DCM module, which formats the data, checks for errors, and performs instantaneous monitoring of the data segment. Each DCM module may include a microprocessor ensuring parallel performance of operations on the data. The ROC device adds auxiliary

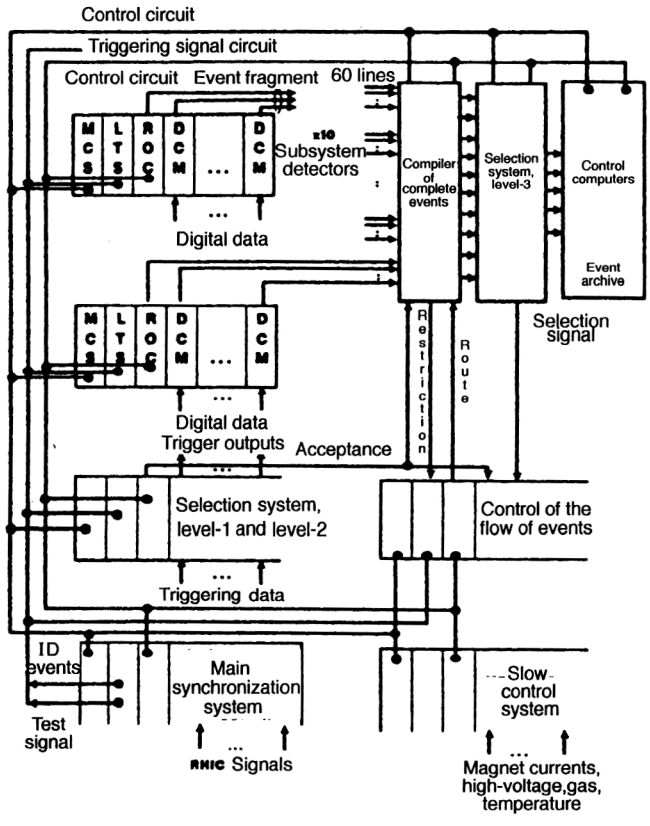

FIG. 33. Block diagram of the DAQ system for PHENIX.

information (the data source, errors, corrections, etc.) to the local data segment and sends it to the event builder. The ROC contains a general-purpose processor, a large memory, and high-speed data transfer channels. It also provides coupling to a network (control net) for performing such operations as loading programs and triggering the setup. The LTS module is designed for synchronization with the accelerator signals, organization of the interaction with the event-selection systems, and control of the event stream.

The complete event is assembled by the event builder. The latter receives data via 60 optical communications lines, and it must ensure a throughput of up to 300 Mbyte/sec. Its design must allow for possible expansion in order to increase its performance. The event builder must deal with many data flows simultaneously and send events via several channels to the level-3 selection device, which consists of a set of 50–100 general-purpose processors. Each processor must possess a high-speed i/o channel and support operating systems and high-level languages. The average decision time must be 50–100 msec/event. The main purpose of the entire selection system is to ensure the processing of all recorded interactions of the Au–Au type and to write them on tape at a rate of less than 20 Mbyte/sec.

The real-time computer system ensures the writing of the selected complete events on tape, monitoring of the operation of the entire setup by the user, and control of the operation of all the local networks. The system should include twelve high-performance work stations.

The STAR setup[95] includes a time-projection chamber (140 000 channels), a silicon vertex detector (72 000 channels), an electromagnetic calorimeter (1200 channels), a system detecting the time of flight (about 8000 channels), and a set of subdetector systems needed for event-triggering of the setup.

Data from the subdetector systems are sent to the DAQ system via optical fibers. The DAQ system must ensure the acquisition of experimental data event by event from each of the detectors, assemble complete events from fragments, write the events on magnetic tape, and distribute them throughout a network for analysis and monitoring of the progress of the experiment (see Fig. 34). The DAQ system is composed of three main parts: the trigger subsystem, the recording subsystem, and the subsystem for real-time information analysis. The trigger system must perform level-1 and 2 event selection in a wide dynamical range from pp to AuAu interactions. Since the event-selection criteria characterizing the state of the quark-gluon plasma are not well known, it must be easy to rearrange the selection system to take into account a change of the selection criteria in the course of an experiment using recent information. The recording subsystem separates the data into fragments accord-

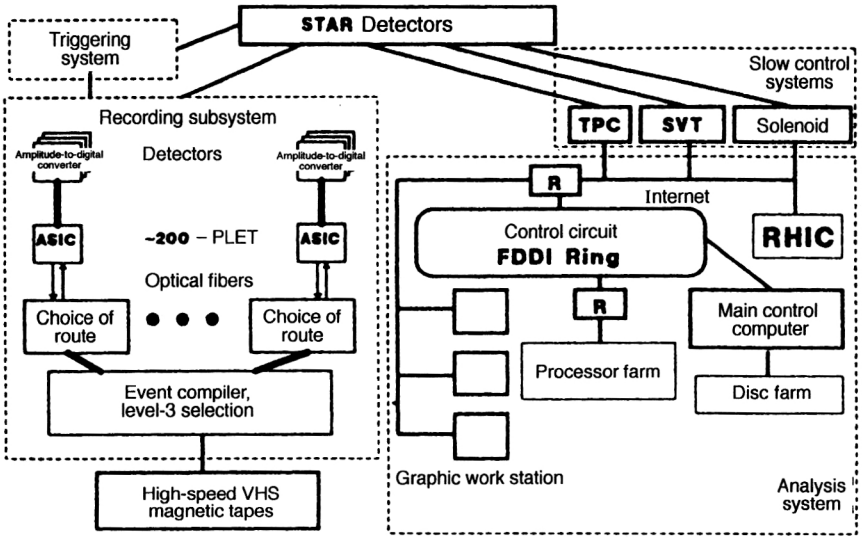

FIG. 34. Block diagram of the DAQ system for the STAR setup (RHIC, Brookhaven).

ing to the subdetector systems. An event-fragment conveyer is formed in the recording modules located near the detectors. An identifier is assigned to each fragment, and is later used to assemble the complete event. Specialized interfaces located behind the modules recording data from a given type of detector ensure the use of a single standard for the subsequent recording stages. On the average, only 10% of the volume of data arriving from the recording modules contains useful information. This makes data compression necessary. In addition, operations are performed to subtract pedestals and correct the enhancement coefficients in each data channel. These operations are performed using ASICs, specialized multiprocessor receiver modules in the VME standard, to which a conveyer feeds event fragments satisfying level-1 and 2 selection criteria. Each of the VME crates of the first level contains a set of 12 receiver modules, modules for connections with other VME crates, and a level-3 event-selection processor (there will eventually be four of them). The connection module, which is a commercially manufactured VME processor module, is responsible for the distribution of processor resources in the crate when working with an individual event and for controlling the interaction with the processors outside that crate. The selection processor performs the track reconstruction within the detector sector connected to the VME crate. Information about the track fragments is sent to the processors of the global VME crate, which take the final decision about choosing the event and writing it on tape. A special processor is used to assemble the complete event. It is responsible for the communications with the coupling processors and controls the transfer of these fragments.

The expected rate at which events appear in collisions of beams of gold ions is 1 kHz, while for proton beams it is 1 MHz. The writing on tape will be limited to rates of 1 Hz and 30 Hz, respectively.

5. DEVICES FOR DATA STORAGE

One of the most important elements of a DAQ system is the data storage system. The amount of data requiring long-term storage reaches several tens of Terabytes (5 Tbytes at DELPHI, 3.4 Tbytes at L3, 5 Tbytes at Zeus, 2.5 Tbytes at H1, 40 Tbytes at D0, and 10 Tbytes at CDF; Ref. 96). In these experiments, the data is mainly written on IBM 3480 cartridges or 5-Gbyte 8-mm Exabyte tapes. The rate of writing information per device is about 0.5 Mbyte/sec (Ref. 97). In most cases the storage rate is less than 5 Mbyte/sec.

In experiments to be performed in the next five years the problem of storing enormous amounts of data will become more severe. The BELLE setup at KEK requires the storage of up to 30 Terabytes of data per year at a high rate (15 Mbyte/sec).[98] The modernized D0 setup will require the storage of about 200 Tbytes at a rate of 25–30 Mbyte/sec. Storage on magnetic tape will still be 4–10 times less expensive than on disks.[99] A special model setup is now being built. It consists of a SONY-DIR 1000M magnetic recorder, ensuring a writing rate of up to 32 Mbyte/sec, with a robot for replacing the magnetic tapes by 24 tapes (up to 2 Tbyte in capacity).[98] A single tape can store up to 42 Gbytes of information.[100]

6. CONCLUSIONS

In this review we have discussed the main changes in the architecture of DAQ systems which have occurred in the last 25 years because of the development of computing technology (computers, interfaces, communications).

The need to simultaneously perform automatic measurements via several data channels has led to the practical use of processors ensuring control over the experiment, fairly simple connection of nonstandard instrumentation, fast response to external interrupt signals, high-speed information transfer, and real-time operation. The use of multichannel detectors in experimental setups has led to the appearance of modular electronics, ensured the possibility of creating local recording subsystems for groups of detectors, with each subsystem performing compression, packing, and preliminary analysis of data by hardware processors, and the creation of multilevel event selection systems.

The appearance of microprocessors and standards for the construction of VME, FASTBUS, etc. open bus systems has allowed the number of data channels to be increased considerably. It has led to the natural development of a DAQ architecture with separate data flows through the detectors, and has simplified the processing procedure at all stages of the information transfer. It has become possible to record events when the volume of data reaches several hundred kilobytes. Means of communication have ensured the transfer of large data flows with operational switching of these flows from many data channels to a set of analyzing processors.

The architecture of any of the current DAQ systems designed for the huge experimental setups used at the largest accelerators contains nearly all the most important methodological solutions to the problem of organizing data acquisition:

1. Splitting of the information about an event into fragments;
2. The association of an identifier with each fragment, which allows subsequent use of the fragment in a network;
3. The introduction of conveyer processing of event fragments;
4. The organization of multilevel event selection;
5. The use of a network of processors, whose number may differ from the number of fragments an event is divided into, to perform the operations of compression, formatting, pedestal subtraction, inclusion of calibration values, and so on;
6. The use of specialized hardware such as processor modules, multi-input memory, and communications for the high-speed transfer of large amounts of data;
7. The organization of high-speed switches for multibit data flows from **n** inputs to **m** outputs;
8. The creation of farms of processors connected to form a network for performing level-3 and higher event selection;
9. User access to data via numerous work stations;
10. The introduction of automated control over the many slowly varying parameters of the setup such as the gas temperature, pressure, and rate of flow in the detectors, the high voltage, and so on;
11. Archival of the events selected by the trigger system, mainly using magnetic tapes with high write density.

Most of the current experimental installations created at physics centers like the JINR Laboratory of High Energy Physics are significantly smaller in scale than the installations designed to operate at colliders. However, their construction to a greater or lesser degree involves many of the methodological principles listed above.

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